1 Introduction to system concepts and components

1.1 Digital system representation

Combinational (no memory)

Sequential (Combinational + memory)

1.2 System Concept

1.3 Digital system components

1.3.1 Functional blocks

1.3.2 Switches

1.3.3 SSI/MSI/LSI

1.3.4 TTL

1.3.5 CMOS

1.3.6 ECL (very high speed)

1.3.7 Logic building block basic configuration

1.3.7.1 TTL

1.3.7.1.1 Totem pole configuration

1.3.7.1.2 Open collector configuration

1.3.7.1.3 Tri-state gates

1.3.8 IC

1.3.8.1 Ideal logic element

Fan-out

1.3.8.2 Physical logic gates

1.3.8.2.1 Power dissipation

1.3.8.2.2 Voltage transfer characteristics (VTC)

1.3.8.2.3 Noise margin

DC: supply power

AC: voltage coupling

1.3.8.2.4 Switching speed and propagation delay

1.3.9 Comparison of logic families

1.3.9.1 Supply voltage

1.3.9.2 Propagation delay

1.3.9.3 Power consumption

1.3.9.4 Noise immunity

1.3.9.5 Fan out capacity

1.3.9.6 Comparison data for TTL sub-families

1.3.10 Galium Arsenide (GaAs) logic family

1.3.11 PLA

1.4 Digital System links

1.4.1 Ideal Wire

1.4.2 Transmission line

1.4.3 Line termination

2 Discrete and Programmable Logic Design

2.1 Logic circuit design (LCD)

2.2 Discrete and programmable logic design

2.3 Programmable logic devise (PLD) circuit

PROM

PAL

2.3.1 PLA input phase splitters

2.3.2 PLA circuit symbolic representation

2.3.3 PLA minimization

Phase-splitter

Folding

Input-decoder

2.3.4 Systematic methods for PLA minimization

2.3.4.1 Quine-McClusky Method

2.3.5 Minimization of multiple output functions

2.3.6 Minimization by elimination of input variables

3 High speed system design consideration

3.1 Power, ground and cross-talk

3.1.1 Grounding considerations

Best: ground plane

Then: Grid

Parallel strips

Braid or copper strip

3.1.2 Power supply considerations

3.1.2.1 Dynamic impedance of Vcc runs

3.1.2.2 Icc drain due to line driving

3.1.2.3 Vcc bypass capacitor for octal driver

3.1.3 Direct cross-talk noise

3.1.3.1 Crosstalk on etched board (PCB)

3.1.3.2 Crosstalk on wires

3.1.3.3 ?

3.1.3.4 Crosstalk amplitude, rise time and coupled length

3.1.3.5 Crosstalk and line termination

3.1.3.6 Termination on bus lines

3.1.3.7 Crosstalk general recommendations

3.2 Thermal considerations

3.2.1 Thermal resistance

3.2.2 High-speed IC thermal considerations

3.2.3 Design for thermal consideration

4 Digital system design

4.1 Digital system structure / analysis

4.1.1 Combinational circuits (no memory)

4.1.1.1 Examples

4.1.1.1.1 Full adder design

Direct use not, and, or ---- Carry faster

Use ex-or ---- Sum Faster

4.1.1.2 Timing considerations in digital circuit

4.1.1.2.1 The "eye"

4.1.1.2.2 Data set-up and hold time

4.1.1.2.3 Race

4.1.1.3 Hazard

4.1.2 ?

4.1.3 Sequential circuits (combinational + memory)

4.1.3.1 Sequential circuit analysis

4.1.3.2 Final state machine (FSM)

4.1.3.3 Asynchronous sequential circuits

4.1.3.4 Synchronous sequential circuits

4.1.3.5 Race in asynchronous sequential circuit

4.1.3.6 Examples of sequential circuits

(1) parallel transfer register

(2) serial shift register

(3) Johnson counter (useful)

(4) Asynchronous counter (ripple counter)

Max. Speed (different delay)

Decoding spikes or "glitches" (more than one output change)

4.1.3.7 Synchronous sequential circuit design

(1) tow-bit up-down counter

(2) op-code generator (sequencer)

(3) message detector

4.1.3.8 Finite memory circuits

(4) Error detector

4.2 Hard ware description language (HDL)

4.2.1 Introduction to VHDL

4.2.2 Programming in VHDL

6.5.3.1.1.2 2-port FF architecture

6.5.3.1.1.3 Scan-set architecture

6.5.3.1.1.4 Multiplexer scan structure

I just take the title from the notes. Copyright belongs to P.C. Chui
Unfortunately, I only have hardcopy of the notes.