

- 1 Introduction to system concepts and components**
 - 1.1 Digital system representation**
 - Combinational (no memory)
 - Sequential (Combinational + memory)
 - 1.2 System Concept**
 - 1.3 Digital system components**
 - 1.3.1 Functional blocks**
 - 1.3.2 Switches**
 - 1.3.3 SSI/MSI/LSI**
 - 1.3.4 TTL**
 - 1.3.5 CMOS**
 - 1.3.6 ECL (very high speed)**
 - 1.3.7 Logic building block basic configuration**
 - 1.3.7.1 TTL**
 - 1.3.7.1.1 Totem pole configuration**
 - 1.3.7.1.2 Open collector configuration**
 - 1.3.7.1.3 Tri-state gates**
 - 1.3.8 IC**
 - 1.3.8.1 Ideal logic element**
 - Fan-out
 - 1.3.8.2 Physical logic gates**
 - 1.3.8.2.1 Power dissipation**
 - 1.3.8.2.2 Voltage transfer characteristics (VTC)**
 - 1.3.8.2.3 Noise margin**
 - DC: supply power
 - AC: voltage coupling
 - 1.3.8.2.4 Switching speed and propagation delay**
 - 1.3.9 Comparison of logic families**
 - 1.3.9.1 Supply voltage**
 - 1.3.9.2 Propagation delay**
 - 1.3.9.3 Power consumption**
 - 1.3.9.4 Noise immunity**
 - 1.3.9.5 Fan out capacity**
 - 1.3.9.6 Comparison data for TTL sub-families**
 - 1.3.10 Gallium Arsenide (GaAs) logic family**
 - 1.3.11 PLA**
 - 1.4 Digital System links**
 - 1.4.1 Ideal Wire**
 - 1.4.2 Transmission line**

1.4.3 Line termination

2 Discrete and Programmable Logic Design

2.1 Logic circuit design (LCD)

2.2 Discrete and programmable logic design

2.3 Programmable logic device (PLD) circuit

PROM

PAL

2.3.1 PLA input phase splitters

2.3.2 PLA circuit symbolic representation

2.3.3 PLA minimization

Phase-splitter

Folding

Input-decoder

2.3.4 Systematic methods for PLA minimization

2.3.4.1 Quine-McClusky Method

2.3.5 Minimization of multiple output functions

2.3.6 Minimization by elimination of input variables

3 High speed system design consideration

3.1 Power, ground and cross-talk

3.1.1 Grounding considerations

Best: ground plane

Then: Grid

Parallel strips

Braid or copper strip

3.1.2 Power supply considerations

3.1.2.1 Dynamic impedance of Vcc runs

3.1.2.2 Icc drain due to line driving

3.1.2.3 Vcc bypass capacitor for octal driver

3.1.3 Direct cross-talk noise

3.1.3.1 Crosstalk on etched board (PCB)

3.1.3.2 Crosstalk on wires

3.1.3.3 ?

3.1.3.4 Crosstalk amplitude, rise time and coupled length

3.1.3.5 Crosstalk and line termination

3.1.3.6 Termination on bus lines

3.1.3.7 Crosstalk general recommendations

3.2 Thermal considerations

- 3.2.1 Thermal resistance
- 3.2.2 High-speed IC thermal considerations
- 3.2.3 Design for thermal consideration

4 Digital system design

4.1 Digital system structure / analysis

4.1.1 Combinational circuits (no memory)

4.1.1.1 Examples

4.1.1.1.1 Full adder design

Direct use not, and, or ---- Carry faster

Use ex-or ---- Sum Faster

4.1.1.2 Timing considerations in digital circuit

4.1.1.2.1 The “eye”

4.1.1.2.2 Data set-up and hold time

4.1.1.2.3 Race

4.1.1.3 Hazard

4.1.2 ?

4.1.3 Sequential circuits (combinational + memory)

4.1.3.1 Sequential circuit analysis

4.1.3.2 Final state machine (FSM)

4.1.3.3 Asynchronous sequential circuits

4.1.3.4 Synchronous sequential circuits

4.1.3.5 Race in asynchronous sequential circuit

4.1.3.6 Examples of sequential circuits

(1) parallel transfer register

(2) serial shift register

(3) Johnson counter (useful)

(4) Asynchronous counter (ripple counter)

Max. Speed (different delay)

Decoding spikes or “glitches” (more than one output change)

4.1.3.7 Synchronous sequential circuit design

(1) tow-bit up-down counter

(2) op-code generator (sequencer)

(3) message detector

4.1.3.8 Finite memory circuits

(4) Error detector

4.2 Hard ware description language (HDL)

4.2.1 Introduction to VHDL

4.2.2 Programming in VHDL

- 4.2.3 VHDL operators**
- 4.2.4 Signal assignment statements**
- 4.2.5 Concurrent statement characteristics**
- 4.2.6 VHDL description of a circuit module**
 - 4.2.6.1 Entity-Architecture pair**
 - 4.2.6.2 One-bit VHDL full adder**
- 4.2.7 VHDL description of a system**
 - 4.2.7.1 Four-bit full adder**
- 4.2.8 VHDL process**
- 4.2.9 The “if-then-else” statement**
- 4.2.10 Modeling Flip-Flops using VHDL “process”**
- 4.2.11 The three models of VHDL**
 - 4.2.11.1 Data-flow model**
 - 4.2.11.2 Structural model**
 - 4.2.11.3 Behavioral model**
 - 4.2.11.4 The Behavioral model of a Edge Triggered D-type flip flop**

5 Digital logic testing and fault detection

- 5.1 Data transfer**
 - 5.1.1 Bus structure**
 - 5.1.2 Bus systems**
- 5.2 Register transfer language (RTL)**
 - 5.2.1 Data transfer description by RTL**
- 5.3 Example of digital design**
 - 5.3.1 Logic unit (LU) design**
 - Universal logic implementer (ULI)
- 5.4 Sequence controller**
 - 5.4.1 Hardwired logic**
 - 5.4.2 Micro-programmed logic**
 - 5.4.3 Micro-sequencer organization**
- 5.5 Bit-sliced micro-processor**
 - 5.5.1 The “bit sliced” data processing unit**
 - 5.5.2 Micro-programmed bit-sliced micro processor**
 - 5.5.3 Characteristics of bit-sliced micro processor**
- 5.6 Memory systems**
 - 5.6.1 Classification of memory systems**
 - 5.6.2 Semiconductor read-write memory (RWM)**
 - DRAM, SRAM

- 5.6.3 The structure of a RWM chip
 - 5.6.4 The structure of a memory system
 - 5.6.4 Sequential access memory (SAM) system
 - 5.6.4.1 FIFO memory system
 - 5.6.4.1.1 FIFO with register (fast, small, simple control)
 - 5.6.4.1.2 FIFO with RAM (slow, large, complex control)
- 6 Design for test (DFT)
 - 6.1 Failure, error and fault
 - 6.2 Testing objective and cost
 - 6.2.1 Testing cases
 - 6.2.1.1 Testing purposes
 - 6.2.1.2 Kinds of test
 - 6.3 Testing overview
 - 6.4 Functional testing
 - 6.4.1 Memory testing
 - 6.4.1.1 Memory faults
 - 6.4.1.2 Memory test patterns
 - 6.4.1.2.1 Traditional test patterns
 - 6.4.1.2.2 Testing time for memory patterns
 - 6.4.1.2.3 Modified algorithmic test sequence (MATS)
 - 6.4.2 Logic testing
 - 6.4.2.1 Logic faults
 - 6.4.2.2 Fault detection
 - 6.4.2.3 Boolean difference
 - 6.4.2.4 Fault detection test set
 - 6.4.2.5 Path sensitization
 - 6.4.3 Compact tests
 - 6.4.3.1 Compact memory tests
 - 6.4.3.1.1 Memory checksum
 - 6.4.3.1.2 Parity check tests
 - 6.4.3.2 Compact logic tests
 - 6.5 Design for testability (DFT)
 - 6.5.1 Testing cost
 - 6.5.2 Controllability and observability
 - 6.5.3 Scan techniques
 - 6.5.3.1 Shift register scan structure
 - 6.5.3.1.1 Implementation
 - 6.5.3.1.1.1 Multiplex data FF architecture

6.5.3.1.1.2 2-port FF architecture

6.5.3.1.1.3 Scan-set architecture

6.5.3.1.1.4 Multiplexer scan structure

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